Amendments to the Claims

Please amend claims 1- 5, 16, 21 and 22 as follows. This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An integrated circuit for electrostatic discharge (ESD) protection comprising:

a silicon-controlled rectifier (SCR) including a ~~first~~ transistor integrally formed with the SCR, ~~wherein~~ the ~~first~~ transistor ~~has~~ including a ~~first~~ gate located over a channel between a first doped region of the SCR and a second doped region of the SCR;

a contact pad coupled to the SCR; and

a control circuit ~~coupled to the silicon-controlled rectifier, wherein the control circuit~~ to change ~~changes a normal~~ a first holding voltage of the SCR to ~~a modified~~ a second holding voltage to keep the SCR in latch-up ~~after~~ in response to detecting ~~a electronic static discharge~~ an ESD event, and ~~changes~~ to change the second ~~modified~~ holding voltage of the SCR to the first ~~normal~~ holding voltage after a time period to keep the SCR from latching-up, ~~latching up;~~ wherein the control circuit is coupled only to the SCR at the second doped region. ~~and~~

~~wherein the first gate of the first transistor is not directly coupled to the control circuit.~~

2. (Previously Presented) The circuit of claim 1, wherein the time period is determined by an RC constant of the control circuit.

3. (Previously Presented) The circuit of claim 1, the control circuit further comprising a resistor, a capacitor and an output terminal of the control circuit disposed between the resistor and the capacitor.

4. (Original) The circuit of claim 1, the control circuit including a resistor-capacitor delay circuit.

5. (Original) The circuit of claim 1, the SCR further comprising a p-type substrate, an n-well an n-well formed in the p-type substrate, a p-type diffused region formed in the n-well, and an n-type diffused region formed outside of the n-well.

6-15. (Canceled)

16. (Currently Amended) An integrated circuit for electrostatic discharge (ESD) protection comprising:

a plurality of contact pads;

a plurality of ~~first~~ silicon-controlled rectifiers (SCR), each ~~of the first~~ SCRs associated with one of the plurality of contact pads, ~~wherein~~ each ~~first~~ SCR including ~~includes~~ ~~first~~ a ~~MOS~~ transistor integrally formed with the SCR,[[;]] wherein for each of the ~~first~~ SCRs, a gate of the ~~first MOS~~ transistor is coupled to the contact pad or ground; and

a plurality of control circuits, ~~wherein a~~ each control circuit coupled to ~~each~~ one of the ~~first~~ SCRs, ~~wherein~~ the control circuit to change ~~changes~~ a ~~normal~~ first holding voltage of the SCR to a ~~modified~~ second holding voltage to keep the SCR in latch-up ~~after~~ in response to detecting an ~~electronic static discharge~~ ESD event, and ~~changing~~ to change the second ~~modified~~ holding voltage of the SCR to the first ~~a normal~~ holding voltage after a time period to keep the SCR from latching-up ~~latching up~~.

17 – 20 (Canceled)

21. (Currently Amended) The circuit of claim 16, wherein the control circuit further comprises ~~comprising~~ a resistor-capacitor delay circuit.

22. (Currently Amended) The circuit of claim 16, ~~the~~ wherein each control circuit comprises ~~further~~ ~~comprising~~ an output terminal coupled to a gate of ~~each of~~ ~~the~~ a p-type and an n-type transistor associated with each SCR ~~transistors~~.

23 – 32 (Canceled)